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09/512,954	02/25/2000	Pablo M. Acosta-Serafini	MIT8072	7604

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EXAMINER	
YE, LIN	

ART UNIT	PAPER NUMBER
2612	8

DATE MAILED: 06/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/512,954	Applicant(s) ACOSTA-SERAFINI ET AL.	
	Examiner Lin Ye	Art Unit 2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19-23* is/are allowed.

6)☐ Claim(s) *1-7 and 11-17* is/are rejected.

7)☒ Claim(s) *8-10 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-23 filed on 4/1/04 have been considered but are moot in view of the new ground(s) of rejection. Since a new ground of rejection is being applied against unamended claims, this action is not made final.

Although a new ground of rejection has been used to address limitations of the claims, a response is considered necessary for one of the applicant's argument since the Lee reference (US Patent Publication 2002/0101528) will continue to be used to meet several of the claimed limitations.

Relative to claim 1, the applicant argues that Lee reference does not teach or suggest the micro-controller 81that is not integrated with an image sensor, and further employs an interface ASIC 82 that is not integrated with an image sensor. The examiner disagrees. The Lee reference clearly states the interface ASIC 82 and controller 81 can also be formed as part of the camera-on-a chip (as same semiconductor substrate) system (10) which including image pixel sensor array 12 a showing Figure 3 (See Page 3 [0037], lines 14-19).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-7 and 11-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. U.S. Publication 2002/0101528 in view of Umeda et al U.S. Patent 6,452,632 and Katsuma U.S. Patent 5,398,123.

Referring to claim 1, the Lee reference discloses in Figure 3, an imager system provided in a semiconductor substrate (camera-on-a chip system 10) comprising: a plurality of photosensitive, charge integrating pixels (pixel array 12, See page 2 [0027]) arranged in rows and columns of a pixel array for capturing illumination of a scene to be imaged, each pixel (APS pixel) comprising a photogenerated charge accumulation region (photodiode) of the substrate and a sense node at which an electrical signal, indicative of pixel charge accumulation, can be measured without discharging the accumulation region (the pixel array 12 can store charges of the indent image , See page 2 [0028]); pixel access control circuitry (pixel addressing 16 and Timing and control 50)connected to pixel array rows and columns to deliver pixel access signals generated by the access control circuitry for independently(See Page 2 [0030]) accessing a selected pixel in the array; integration control circuitry (Interface ASIC 82 and micro-controller 81) connected to access a selected pixel of the array to read the sense node electrical signal of the selected pixel, and configured to generated pixel-specific integration (setting exposure conditions) control signals delivered to the selected pixel, independent of other pixels (The CMOS active sensor APS pixel can independent control and accessing by row addressing and column addressing circuit, see Col. 4, lines 16-19 and lines 25-31); and an output interface circuit (Data storage

/Formatter 85, see page 3 [0037]) connected to the pixel array to produce output image data based on sense node electrical signals form the pixel array. The Lee reference also shows the integration control circuitry (81) generates integration control signals based on the input signals provided by Human and Camera Control Interface. However, it does not explicitly states the Human and Camera Control Interface can also be formed as part of the camera-on-a chip (as same semiconductor substrate) system (10).

The Umeda reference discloses in Figure 1, a single solid state image sensor chip includes an area sensor section (102), digital signal processor section (107) and interface section (108) that used to execute the command input operation and also as function of outputting digital video data output from image sensor (See Col. 9, lines 31-38). The Umeda reference is an evidence that one of ordinary skill in the art at the time to see more advantages for area sensor section, digital signal processor section and interface section into a single chip, because it will significantly reduce the device size and making the device more portable. For that reason, it would have been obvious to see the Human and Camera Control Interface can also be formed as part of the camera-on-a chip system (10) disclosed by Lee.

The Lee and Umeda referenced do not explicitly show the input interface circuit connected to accept a dynamic range specification input for the array pixels.

The Katsuma reference discloses in Figure 1, an imager system including an input interface circuit section (I/o for setting parameter 6 and parameter memory 4) for accepting a dynamic range specification (0 to 2.0, 0 to 2.5 or 0 to 3.0) input (by operator selects) for the array sensor (CCD scanner 18) (See Col. 5, lines 22-38). The

Umeda reference is evidence that one of ordinary skill in the art at the time to see more advantages for the imager system can accept a dynamic range specification input by operator so that it is able to obtain an image with visually favorable quality (See Col. 1, lines 60-65). For that reason, it would have been obvious to see the input interface circuit connected to accept a dynamic range specification input for the array pixels disclosed by Lee

Referring to claim 2, the Umeda reference discloses wherein the pixel sense node (capacitances 32-1, 32-2) electrical signal comprises a voltage signal as shown in Figure 90 (See Col. 29, lines 59-64).

Referring to claim 3, the both of Lee and Umda references disclose wherein the charge integrating (exposure) pixels comprise CMOS pixels.

Referring to claim 4, the Lee reference discloses wherein the pixel-specific integration control signals generated by the integration controller comprise pixel-specific charge accumulation reset signals (See Page 2, [0030]).

Referring to claim 5, the Lee reference discloses the imager system comprising an array of memory cells (buffer memory 85, see Page 3 [0037]), each memory cell corresponding to a specified pixel in the pixel array and connected to store from the integration controller an indication of number of reset occurrences of the specified.

Referring to claim 6, the Lee reference discloses the memory cell array (buffer memory 85) is configured spatially separate from the pixel array (12) as shown in Figure 3

Referring to claim 7, the Lee reference discloses wherein the output interface circuit (85) comprises a image data **formatter** configured to generated output image

data based on sense node electrical signals from the pixel array and corresponding reset occurrence data from the memory cell array (buffer memory of 85) as shown in Figure 3.

Referring to claim 11, the Lee reference discloses in Figure 1, the image system comprising a plurality of CMOS circuits, and an output interface circuit (18) coupled CDS, PGA, ADC circuits.

Referring to claim 12, the Lee reference discloses the output interface circuit (18) further comprises an analog-to-digital converter (ADC) configured to digitize sense node electrical signals from the pixel array.

Referring to claim 13, the Lee reference discloses in Figure 5, wherein the analog-to-digital converter (ADC 128) comprises an array of analog-to-digital converter (See page 3, [0041]); and further comprising a multiplexer (126) connected between the pixel array and the analog-to-digital converter array for directing a selected sense node electrical signal from the pixel array to a selected converter in the array of converters.

Referring to claim 14, the Lee, Umda and Katsuma references disclose all subject matter as discussed with respected to same comment as with claim 1.

Referring to claim 15, the Lee, Umda and Katsuma references disclose all subject matter as discussed with respected to same comment as with claim 1.

Referring to claim 16, the Lee, Umda and Katsuma references disclose all subject matter as discussed with respected to same comment as with claim 1.

Referring to claim 17, the Lee, Umda and Katsuma references disclose all subject matter as discussed with respected to same comment as with claim 1.

Allowable Subject Matter

4. Claims 8-10 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Referring to claim 20, the prior art does not teach or fairly suggest the integration controller comprises a comparator circuit corresponding to each column of the pixel array, each comparator circuit connected to compare a sense node electrical signal of a pixel selected from the corresponding array column with a reference electrical signal that is generated based on the dynamic range specification input to produce a comparator output signal determinative of reset timing of the selected pixel.

5. Claims 19-23 allowed.

Referring to claim 19, the prior art does not teach or fairly suggest a method wherein providing a plurality of integration slots for the integration period, all **integration slots** ending with integration period start, and each integration slot following the first slot being of **successively shorter duration**; initiating charge integration of each pixel in the pixel array for the integration period and the first integration slot; for any current integration slot except a last integration slot, at an intermediate time during the current integration slot, evaluating the sense node electrical signal of each pixel for which the current integration slot was initiated to determine if that pixel will saturate during the current integration slot, the saturation evaluation based on the electrical signal range characteristic of that pixel and the ration of duration of a next succeeding integration slot to duration of the current

integration indicates pixel saturation during the current integration slot; resetting any pixel for which the integration evaluation indicates pixel saturation during the current integration slot; permitting continued integration to the end of the current integration slot of any pixel for which the integration evaluation does not indicate saturation during the current integration slot, and initiating a next succeeding integration slot for any reset pixel; repeating steps until the end of the integration period and the last integration slot is reached; and producing output image data for each pixel based on sense node electrical signals from that pixel and indication of number of integration slots for which that pixel was initiated during the integration period

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
   a. Sivlerbrook U.S 6,614,560 discloses an imager system provided in a semiconductor substrate (48) as shown in Figure 15.
   b. Hirt et al. U.S 5,883,830 discloses the CMOS image-sensing device includes, on one integrated circuit, a sensor array and compensation circuitry.
   c. McCaffrey et al. U.S. 6,101,294 discloses an imager can adjust integration period based on previous integration period

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Lin Ye** whose telephone number is **(703) 305-3250**.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy R Garber can be reached on (703) 305-4929.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, DC. 20231

Or faxed to:

(703) 872-9306

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal drive, Arlington, VA., Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

WENDY R. GARBER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

Lin Ye
June 8, 2004